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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/496,794	02/02/2000	John T. Moore	MICT-0005-D1-US	6700
21906	7590	03/09/2006	EXAMINER	
TROP PRUNER & HU, PC 8554 KATY FREEWAY SUITE 100 HOUSTON, TX 77024			OWENS, DOUGLAS W	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

Claim Rejections - 35 USC § 102/103

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 26 is rejected under 35 U.S.C. 102(b)/103(a) as being anticipated by US Patent No. 5,763,932.

Regarding claim 1, Pan et al. teach a semiconductor structure (Figs. 13 and 14), comprising;

a support (42);

a first material (46) deposited on said support, said first material having a first etch rate;

a trench formed through said first material and into the support (Fig. 10); and

a trench filler material (74) deposited in the trench, the trench filler material having an etch rate that is less than 1.2 times the first etch rate and substantially similar to the first etch rate (Col. 5, line 65 – Col. 6, line 3), the semiconductor structure having a planar upper surface formed of the first material and the trench filler material (Fig. 13).

Alternatively in the final structure, Pan et al. teach a first material (44) on the support, wherein the first material and the trench filler material have the same etch rate,

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since they are both TEOS oxides. In the alternative, Pan et al. do not show that the trench filler and first material have an exposed planar surface. Pan et al. teach that “it would be desirable to develop a method of forming a field isolation region with a substantially flat upper surface, without the requirement of the extra masking step required to form photoresist block...” (Col. 2, lines 42 – 45). It would have been obvious to one of ordinary skill in the art to planarize the final structure, since it is desirable to form a substantially flat upper surface.

Claim Rejections - 35 USC § 103

3. Claims 27 – 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan et al.

Regarding claim 27, Pan et al. teaches a semiconductor structure, wherein the first material includes silicon dioxide deposited from tetraethyorthosilicate.

Regarding claim 28, Pan et al. teaches a semiconductor structure, wherein the first material includes silicon dioxide deposited by chemical vapor deposition (Col. 4, lines 25 – 28).

Regarding claim 29, Pan et al. teaches a semiconductor structure, wherein the first material includes silicon dioxide deposited from tetraethyorthosilicate.

Regarding claim 30, Pan et al. teaches a semiconductor structure, wherein the first material includes silicon dioxide deposited by chemical vapor deposition (Col. 5, lines 45 – 48).

Response to Arguments

4. Applicant's arguments filed March 7, 2005 have been fully considered but they are not persuasive.

Applicant argues that Pan et al. do not teach the semiconductor structure having a planar exposed upper surface formed of the first material and the trench filler material. This feature can be seen in Fig. 13, or alternatively, it would have been obvious to planarize the surface (44, 74) as explained above.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

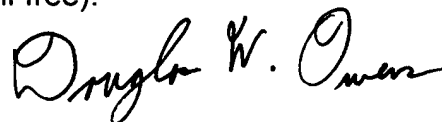
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, reading "Douglas W. Owens". The signature is written in a cursive, flowing style.

Douglas W Owens
Examiner
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